****Name:Xunzhi Li****

****ID:10457500****

****#11.5** “ As described in the text, the PCI-Express bus consists of thirty-two “lanes“. As of January 2009, each lanes is capable of the maximum data rate of 500 MB per second. Lanes are allocated to a device 1,2,3,8,16 , or 32 lanes at a time.**

**Assume that a PCI-Express bus is to be connected to a high-definition video card that is supporting a 1920 x 1080 true color (3 bytes per pixel) progressive scan monitor with a refresh rate of 60 frames per second. How many lanes will this video card require to support the monitor at full capability?**”

60\*1920\*1080\*3=373248000 bytes = 373.25 MB < 500 MB

So one lane is enough to support the monitor.

****Exercise C)****

**Find a current computer ad in a magazine or newspaper or online. Identify each of the future items in the ad, show its position in the system block diagram in Figure 11.1 (on page # 336 -5th edition textbook), explain how it operates, and define its purpose.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Model number** | **sSpec number** | **Cores (threads)** | **Frequency** | **[Turbo](https://en.wikipedia.org/wiki/Intel_Turbo_Boost" \o "Intel Turbo Boost)** | **[L2 cache](https://en.wikipedia.org/wiki/CPU_cache" \l "Multi-level_caches" \o "CPU cache)** | **[L3 cache](https://en.wikipedia.org/wiki/CPU_cache" \l "Multi-level_caches" \o "CPU cache)** | **I/O bus** |
| [Core i7-9700K](https://ark.intel.com/content/www/us/en/ark/compare.html?productIds=186604) | * SRELT (P0) * SRG15 (R0) | 8 (8) | 3.6 GHz | 10/10/10/11/11/12/12/13 | 8 × 256 KiB | 12 MiB | DMI 3.0 |